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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,372	12/29/2000	Anthony X. Jarvis	00-BN-051 (STMI01-00051)	8275

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,372	JARVIS ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

2. In view of the Appeal Brief filed on 28 October 2004, PROSECUTION IS HEREBY REOPENED. Please see the rejection set forth below.

3. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

4. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Papers Submitted

5. It is hereby acknowledged that the following papers have been received and placed on record in the file: Notice of Appeal filed 26 August 2004; One Month Extension of Time field 26 August 2004; and Appeal Brief filed 28 October 2004.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greenley, U.S. Patent No. 5,761,469 (herein referred to as Greenley) in view of Zaidi, U.S. Patent Number 5,619,668 (herein referred to as Zaidi).

8. Regarding claims 1 and 14, taking claim 14 as exemplary, Greenley has taught a processing system comprising:

a. A data processor (Greenley 100 of Fig.1).

b. A memory coupled to said data processor (Greenley Col.1 lines 41-43).

c. Wherein said data processor comprises:

i. An instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline (Greenley Col.1 lines 34-40).

ii. A data cache (Greenley 180 of Fig.1) capable of storing data values used by said pending instruction (Greenley Col.1 lines 42-43).

iii. A plurality of registers (150 of Fig.1) capable of receiving said data values from said data cache (Greenley Col.1 lines 41-45).

iv. A load store unit (Greenley 130 of Fig.1) capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation (Greenley Col.1 lines 15-21, 63-67 and Col.2 lines 1-7, 13-15).

v. A shifter circuit (Greenley 160,170 of Fig.1) associated with said load store unit capable of one of a) shifting (Greenley Col.2 lines 19-31), b)

sign extending (Greenley Col.2 lines 48-54), and c) zero extending (Greenley Col.2 lines 45-47) said first data value prior to loading said first data value into said target register.

9. Greenley has not explicitly taught

a. A plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor; and

b. Bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

10. However, Greenley has taught a sign extension unit (Greenley 160 of Fig.1) that fills in unoccupied bits of a register by extending its sign after it is loaded from the data cache (Greenley Col.2 lines 48-50). Zaidi has taught this as well (Zaidi column 8, lines 6-52) and

a. A plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor (Zaidi column 1, line 63 to column 2, line 10); and

b. Bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit (Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5).

11. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Zaidi, the bypass increases the speed of microprocessors (Zaidi

column 2, lines 33-34), by eliminating the time required to read data from the registers and aligning the data, and reduces the need to stall pipelines (Zaidi column 2, lines 35-37), by eliminating the need for the pipeline to stall, i.e. delay execution, until the data is ready to be read from the registers and aligned properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the bypass of Zaidi in the device of Greenley to increase processor speed.

12. Claim 1 is nearly identical to claim 14. Claim 1 differs in its lack of a main memory and memory-mapped peripheral circuits, but comprises the same data processor as claim 14, and is therefore rejected for the same reasons.

13. Regarding claims 2 and 15, taking claim 15 as exemplary, Greenley in view of Zaidi has taught the processing system as set forth in claim 14, wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation (see above rejection of claim 1, as well as Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5). While Greenley has taught a different register size than the applicant (Greenley Col.2 lines 17-19), the situation when a register has no unoccupied bits after being loaded with data from a data cache remains the same, with the size of the register and word being moot. Therefore Greenley's loading of a double word has the same consequences as the applicant's loading of a word.

14. Claim 2 is nearly identical to claim 15. Claim 2 differs in its parent claim, but comprises the same data processor as claim 15, and is therefore rejected for the same reasons.

15. Regarding claims 3 and 16, taking claim 16 as exemplary, Greenley in view of Zaidi has taught the data processor as set forth in claim 15, wherein said bypass circuitry (Zaidi column 5,

lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5) transfers said first data value from said data cache directly to said target register at the end of two machine cycles (Greenley Col.4 lines 17-20).

16. Claim 3 is nearly identical to claim 16. Claim 3 differs in its parent claim, but comprises the same data processor as claim 16, and is therefore rejected for the same reasons.

17. Regarding claims 4 and 17, taking claim 17 as exemplary, Greenley in view of Zaidi has taught the data processor as set forth in claim 14, wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation (see Greenley Col.2 lines 17-20, 24-30, 46-47).

18. Claim 4 is nearly identical to claim 17. Claim 4 differs in its parent claim, but comprises the same data processor as claim 17, and is therefore rejected for the same reasons.

19. Regarding claims 5 and 18, taking claim 18 as exemplary, Greenley in view of Zaidi has taught the data processor as set forth in claim 17, wherein said shifter circuit loads said shifted first data value into said target register at the end of two machine cycles (Greenley Col.4 lines 17-20), but has not explicitly taught the load taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as when the data is already properly aligned since it is coming from the data cache, which only contains aligned data, or from the ALU, which outputs aligned data, the data processor as configured above will execute the load instruction at least one cycle faster due to the elimination of the alignment operations (Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5). This

will create a latency of at least one cycle fewer for those load instructions which bypass the sign extension unit, and at least one more cycle for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Zaidi have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Zaidi (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

20. Claim 5 is nearly identical to claim 18. Claim 5 differs in its parent claim, but comprises the same data processor as claim 18, and is therefore rejected for the same reasons.

21. Regarding claims 6 and 19, taking claim 19 as exemplary, Greenley in view of Zaidi has taught the data processor as set forth in claim 14, wherein said shifter circuit one of a) shifts, b) sign extends, and c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation (see Greenley Col.2 lines 17-20, 36-40, 46-47).

22. Claim 6 is nearly identical to claim 19. Claim 6 differs in its parent claim, but comprises the same data processor as claim 19, and is therefore rejected for the same reasons.

23. Regarding claims 7 and 20, taking claim 20 as exemplary, Greenley in view of Zaidi has taught the data processor as set forth in claim 6, wherein said shifter circuit loads said shifted first data value into said target register at the end of two machine cycles (Greenley Col.4 lines 17-20), but has not explicitly taught the transfer taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as when the data is already properly aligned

since it is coming from the data cache, which only contains aligned data, or from the ALU, which outputs aligned data, the data processor as configured above will execute the load instruction at least one cycle faster due to the elimination of the alignment operations (Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5). This will create a latency of at least one cycle fewer for those load instructions which bypass the sign extension unit, and at least one more cycle for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Zaidi have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Zaidi (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

24. Claim 7 is nearly identical to claim 20. Claim 7 differs in its parent claim, but comprises the same data processor as claim 20, and is therefore rejected for the same reasons.

25. Regarding claims 8, 9, 21, and 22, taking claims 21 and 22 as exemplary, Greenley in view of Zaidi has taught the data processor as set forth in claim 14, but Greenley has not explicitly taught

a. Wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache; and

b. Wherein said multiplexer has a second input channel coupled to an output of said shifter circuit.

26. However, Greenley has taught a sign extension unit (Greenley 160 of Fig.1) that fills in unoccupied bits of a register by extending its sign after it is loaded from the data cache (Greenley Col.2 lines 48-50). Zaidi has taught this as well (Zaidi column 8, lines 6-52) and

a. Wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache (Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5); and

b. Wherein said multiplexer has a second input channel coupled to an output of said shifter circuit (Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5).

27. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Zaidi, the bypass increases the speed of microprocessors (Zaidi column 2, lines 33-34), by eliminating the time required to read data from the registers and aligning the data, and reduces the need to stall pipelines (Zaidi column 2, lines 35-37), by eliminating the need for the pipeline to stall, i.e. delay execution, until the data is ready to be read from the registers and aligned properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the bypass of Zaidi in the device of Greenley to increase processor speed.

28. Claims 8 and 9 are nearly identical to claims 21 and 22 respectively. Claims 8 and 9 differ in its parent claim, but comprises the same data processor as claims 21 and 22, and is therefore rejected for the same reasons.

29. Regarding claim 10, Greenley has taught for use in a processor comprising an N-stage execution pipeline (Greenley Col.1 lines 34-40), a data cache (Greenley 180 of Fig.1), and a plurality of registers (Greenley 150 of Fig.1), a method of loading a first data value from the data cache into a target one of the registers, the method comprising the steps of:

a. Determining if a pending instruction in the execution pipeline is one of a load word operation, a load half-word operation, and a load byte operation (Greenley Col.1 lines 63-67, Col.2 lines 1-7, 17-19 and Col.5 lines 13-24).

b. In response to a determination that the pending instruction is a load half-word operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register (Greenley Col.2 lines 24-31).

c. In response to a determination that the pending instruction is a load byte operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register (Greenley Col.2 lines 35-40).

30. Greenley has not explicitly taught where in response to a determination that the pending instruction is a load word operation, transferring the first data value from the data cache directly to the target register without processing the first data value in the shifter circuit. However, Greenley has taught a sign extension unit (Greenley 160 of Fig.1) that fills in unoccupied bits of a register by extending its sign after it is loaded from the data cache (Greenley Col.2 lines 48-50). Zaidi has taught this as well (Zaidi column 8, lines 6-52) and where in response to a determination that the pending instruction is a load word operation, transferring the first data

value from the data cache directly to the target register without processing the first data value in the shifter circuit (Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Zaidi, the bypass increases the speed of microprocessors (Zaidi column 2, lines 33-34), by eliminating the time required to read data from the registers and aligning the data, and reduces the need to stall pipelines (Zaidi column 2, lines 35-37), by eliminating the need for the pipeline to stall, i.e. delay execution, until the data is ready to be read from the registers and aligned properly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the bypass of Zaidi in the device of Greenley to increase processor speed.

31. Regarding claim 11, Greenley in view of Zaidi has taught the method as set forth in claim 10, wherein the step of transferring the first data value requires two machine cycles during a load word operation (Greenley Col.4 lines 17-20). While Greenley has taught a different register size than the applicant (Greenley Col.2 lines 17-19), the situation when a register has no unoccupied bits after being loaded with data from a data cache remains the same, with the size of the register and word being moot. Therefore Greenley's loading of a double word has the same consequences as the applicant's loading of a word (*In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

32. Regarding claim 12, Greenley in view of Zaidi has taught the method as set forth in claim 10, wherein the step of transferring the first data value requires two machine cycles during a load half-word operation (Greenley Col.4 lines 17-20), but has not explicitly taught the transfer taking three machine cycles. However, Greenley has taught this two-cycle latency for all load

instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as when the data is already properly aligned since it is coming from the data cache, which only contains aligned data, or from the ALU, which outputs aligned data, the data processor as configured above will execute the load instruction at least one cycle faster due to the elimination of the alignment operations (Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5). This will create a latency of at least one cycle fewer for those load instructions which bypass the sign extension unit, and at least one more cycle for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Zaidi have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Zaidi (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

33. Regarding claim 13, Greenley in view of Zaidi has taught the method as set forth in claim 10 wherein the step of transferring the first data value requires two machine cycles during a load byte operation (Greenley Col.4 lines 17-20), but has not explicitly taught the transfer taking three machine cycles. However, Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension. In the situation where the load instruction fills the target register completely and no sign extension is needed, such as when the data is already properly aligned since it is coming from the data cache, which only contains aligned data, or from the ALU, which outputs aligned data, the data processor as configured above will

execute the load instruction at least one cycle faster due to the elimination of the alignment operations (Zaidi column 5, lines 17-47; column 8, line 53 to column 9, line 5; column 9, line 57 to column 10, line 3; Figure 2; and Figure 5). This will create a latency of at least one cycle fewer for those load instructions which bypass the sign extension unit, and at least one more cycle for those which need sign extension, such as half-word load instructions. Because the applicant's claimed load instructions, which take 2 and 3 cycles for bypassed and sign-extended instructions, respectively, have no claimed advantages over the 1 and 2 cycles that Greenly in view of Zaidi have taught, but are merely a change in the magnitude of latency, they are considered to be equivalent and thus taught by Greenley in view of Zaidi (see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955)).

Response to Arguments

34. Applicant's arguments, see Appeal Brief, filed 28 October 2004, with respect to the rejection(s)of claim(s) 1-22 under Greenley, U.S. Patent No. 5,761,469 in view of Dye, U.S. Patent Number 6,412,061 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the above.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
6 January 2005

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